## ABSTRACT OF THE DISCLOSURE

An analog-to-digital converter with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution includes a plurality of stages, each stage having a circuit for converting an analog local signal into a digital local signal with a local resolution lower than the predefined resolution, a circuit for determining an analog residue indicative of a quantization error of the converting circuit, a circuit for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and a circuit for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain. The combining circuit includes, for at least one of the stages, a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and a circuit for controlling the digital weight according to the digital correction signal.

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